PATENT COOPERATION TREATY

PCT

INTERNATIONAL PRELIMINARY REPORT ON PATENTABILITY

(Chapter II of the Patent Cooperation Treaty)

(PCT Article 36 and Rule 70)

Applicant's or agent's file reference 12577060/DH/gjm	**FOR FURTHER ACTION**	See Form PCT/IPEA/416
International application No. **PCT**/AU2005/000313	International filing date *(day/month/year)* 4 March 2005	Priority date *(day/month/year)* 5 March 2004

International Patent Classification (IPC) or national classification and IPC

Int. Cl.

G01R 31/3183 (2006.01)

Applicant

VISION FIRE & SECURITY PTY LTD et al

1. This report is the international preliminary examination report, established by this International Preliminary Examining Authority under Article 35 and transmitted to the applicant according to Article 36.
2. This REPORT consists of a total of 3 sheets, including this cover sheet.
3. This report is also accompanied by ANNEXES, comprising:
   a. [X] *(sent to the applicant and to the International Bureau)* a total of **2** sheets, as follows:
      - [X] sheets of the description, claims and/or drawings which have been amended and are the basis for this report and/or sheets containing rectifications authorized by this Authority (see Rule 70.16 and Section 607 of the Administrative Instructions).
      - [ ] sheets which supersede earlier sheets, but which this Authority considers contain an amendment that goes beyond the disclosure in the international application as filed, as indicated in item 4 of Box No. I and the Supplemental Box.

   b. [ ] *(sent to the International Bureau only)* a total of (indicate type and number of electronic carrier(s)) , containing a sequence listing and/or table related thereto, in electronic form only, as indicated in the Supplemental Box Relating to Sequence Listing (see Section 802 of the Administrative Instructions).

4. This report contains indications relating to the following items:

[X]	Box No. I	Basis of the report
[ ]	Box No. II	Priority
[ ]	Box No. III	Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
[ ]	Box No. IV	Lack of unity of invention
[X]	Box No. V	Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
[ ]	Box No. VI	Certain documents cited
[ ]	Box No. VII	Certain defects in the international application
[ ]	Box No. VIII	Certain observations on the international application

Date of submission of the demand	Date of completion of this report
22 December 2005	17 July 2006
Name and mailing address of the IPEA/AU AUSTRALIAN PATENT OFFICE PO BOX 200, WODEN ACT 2606, AUSTRALIA E-mail address: pct@ipaustralia.gov.au Facsimile No. (02) 6285 3929	Authorized Officer **DEREK BARNES** Telephone No. (02) 6283 2198

INTERNATIONAL PRELIMINARY REPORT ON PATENTABILITY

International application No.
PCT/AU2005/000313

Box No. I Basis of the report

1. With regard to the **language**, this report is based on:

[X] The international application in the language in which it was filed

[ ] A translation of the international application into , which is the language of a translation furnished for the purposes of:

[ ] international search (under Rules 12.3(a) and 23.1 (b))

[ ] publication of the international application (under Rule 12.4(a))

[ ] international preliminary examination (Rules 55.2(a) and/or 55.3(a))

2. With regard to the **elements** of the international application, this report is based on *(replacement sheets which have been furnished to the receiving Office in response to an invitation under Article 14 are referred to in this report as "originally filed" and are not annexed to this report)*:

[ ] the international application as originally filed/furnished

[X] the description:

pages **1 to 32** as originally filed/furnished
pages* received by this Authority on with the letter of
pages* received by this Authority on with the letter of

[X] the claims:

pages **33 to 38** as originally filed/furnished
pages* as amended (together with any statement) under Article 19
pages* **39 and 40** received by this Authority on **22 December 2005** with the letter of **the same date**
pages* received by this Authority on with the letter of

[X] the drawings:

pages **1 to 3** as originally filed/furnished
pages* received by this Authority on with the letter of
pages* received by this Authority on with the letter of

[ ] a sequence listing and/or any related table(s) - see Supplemental Box Relating to Sequence Listing.

3. [ ] The amendments have resulted in the cancellation of:

[ ] the description, pages
[ ] the claims, Nos.
[ ] the drawings, sheets/figs
[ ] the sequence listing *(specify)*:
[ ] any table(s) related to the sequence listing *(specify)*:

4. [ ] This report has been established as if (some of) the amendments annexed to this report and listed below had not been made, since they have been considered to go beyond the disclosure as filed, as indicated in the Supplemental Box (Rule 70.2(c)).

[ ] the description, pages
[ ] the claims, Nos.
[ ] the drawings, sheets/figs
[ ] the sequence listing *(specify)*:
[ ] any table(s) related to the sequence listing *(specify)*:

* *If item 4 applies, some or all of those sheets may be marked "superseded."*

Box No. V **Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement**

1. Statement

Novelty (N)	Claims	**3, 4, 9, 13, 17 to 19, 36**	**YES**
	Claims	**1, 2, 5 to 8, 10 to 12, 14 to 16, 20 to 35**	**NO**
Inventive step (IS)	Claims	**nil**	**YES**
	Claims	**1 to 36**	**NO**
Industrial applicability (IA)	Claims	**1 to 36**	**YES**
	Claims	**nil**	**NO**

2. Citations and explanations (Rule 70.7)

NOVELTY (N)

D1: WO 2003/048794 A1 (INTELLITECH CORP.) 12 June 2003

D1 discloses a method and apparatus for embedded built-in self-test of electronic circuits and systems. A set of test vectors is established and after synchronisation is applied to an embedded electronic circuit via an IEEE 1149.1 bus. The resulting output vectors are analysed and results are obtained for diagnosis of the circuit. The test is delayed by a predefined period so that stable results can be obtained. Therefore D1 discloses all of the features of Claims 1, 2, 5 to 8, 10 to 12, 14 to 16, and 20 to 35.

INVENTIVE STEP (IS)

D2: WO 2000/067164 A1 (MENTOR GRAPHICS CORP.) 9 November 2000

D3: US 5,642,057 A (OKE et al) 24 June 1997

D2 discloses a method and apparatus for creating testable circuit designs having embedded cores by applying test vectors to the circuit design.

D3 discloses a testable embedded microprocessor where the embedded microprocessor is isolated and test vectors are applied that have already been developed for the stand-alone microprocessor.

The additional definition of the environment of the embedded system does not involve an inventive step over the cited prior art of D1. Therefore claims 3, 4, 13 and 17 do not involve an inventive step.

The protocols defined in claim 9 are well known in the art. Therefore claim 9 does not involve an inventive step.

The logging of test results is a normal operation in testing and does not involve an inventive step. Therefore claims 18 and 19 do not involve an inventive step.

D2 and D3 do not specifically disclose the use of predefined timing, this can however be taken from the disclosure of D1 and it would be obvious to a person skilled in the art to combine the teachings of D1 with either of D2 or D3. Claims 6, 8, 15 to 24 and 27 to 35 do not involve an inventive step.

Claim 36 does not involve an inventive step for the reasons given for claims 3 and 4.

26. A computer readable data storage medium including the computer program claimed in claim 25 stored thereon.

27. An embedded device testing system for comparing actual device under test input/output vector pairs with modelled device under test input/output vector pairs, wherein actual device under test output vectors are sampled in accordance with a predefined timing reference.

28. The embedded device testing system claimed in claim 27, wherein the predefined timing reference includes a predetermined delay period for each one of said actual device under test input test vectors.

29. The embedded device testing system claimed in claim 28, wherein the predetermined delay for each one of said actual device under test input test vectors is substantially the length of time before the corresponding output vector stabilises.

30. A process for testing an embedded device under test, including the steps of: comparing actual device under test input/output vector pairs with modelled device under test input/output vector pairs, wherein actual device under test output vectors are sampled in accordance with a predefined timing reference.

31. The process claimed in claim 30, wherein the predefined timing reference includes a predetermined delay period for each one of said actual device under test input test vectors.

32. The process claimed in claim 31, wherein the predetermined delay for each one of said actual device under test input test vectors is substantially the length of time before the corresponding output vector stabilises.

33. Apparatus for testing a device under test , including:

(a) means for applying a test input vector to the device under test; and

(b) means for sampling an output vector from the device under test in response to said input vector,

wherein the wherein said sampling is effected in accordance with a predefined timing reference.

34. The apparatus claimed in claim 35, wherein the predefined timing reference includes a predetermined delay period.

35. The apparatus claimed in claim 34, wherein the predetermined delay is substantially the length of time before the corresponding output vector stabilises.

36. A logical connection port for an embedded device testing system, the testing system comprising apparatus adapted to compare actual device under test (DUT) input/output vector pairs with modelled DUT input/output vector pairs, wherein the logical connection port is adapted to indicate a predefined timing reference for determining a point in time at which to sample an output vector as the corresponding output vector in an input/output vector pair;

wherein the logical connection port resides in a DUT model;

wherein the sampled output vector comprises an actual vector of one or more of:

a smoke detector;

a fire detector;

a security device;

a medical device;

a biological tissue processing device; and

an industrial process device; and

wherein the predefined timing reference may comprise one of:

one delay period being a delay period common to all input test vectors, and;

a predetermined delay period for each input test vector.